BSUCA12 Pipelined Processor

Must be submitted electronically by Midnight on Monday, April 30.

IMPORTANT: *Please get started early! That way, when problems arise (which they will!), you will have time to ask for help.*

In this part of the project, you will pipeline the processor that you built as a single cycle. As part of this project, you will demonstrate that your design works correctly in ModelSim and show how fast it can execute a test program that will be provided for you.

This processor has the exact same requirements, as far as functionality is concerned, as the previous part of the project. It must implement the specified ISA. The new twist is that you must pipeline your processor into at least 5 stages.

Data Hazards:
Whenever data bypassing is possible, you must use it to avoid data hazards. If a stall is inevitable, the hardware is responsible for managing the stall (inserting a bubble in the pipeline).

Control Hazards:
When you encounter a branch or jump, you should consider higher performance options, such as: finding out (or resolving) whether the branch is taken or not taken earlier in the pipeline; computing the taken PC (address of the branch target) earlier in the pipeline; use, at most, a one-cycle stall penalty for each branch instruction; adding a simple branch predictor (branch not taken). Points earned will be based upon the performance of your implementations and how did you handle these hazards. If you decide that your implementation will wait until the condition is resolved before fetching another instruction, your project will be graded less 15% of all possible points.

Grading:
You will be awarded bonus credit of up to 50 points for implementing and properly demonstrating a functional cache line to the data memory.

You will be signing up for a 30-miute demo to the instructor/TA during the first week of May. You are welcome to do this anytime earlier assuming that you submitted your project 24-hours ahead.

Submit this assignment in the same way in which you submitted project part 04. You must name your high-level file BSUCA12.v there are no other file naming restrictions.