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Part 5 – Pipelined Data Path

Control Table:

Operation	OpCode	RegDst	RegWrite	ALUSrc	ALUOp	MemWrite	MemToReg	PCSrc	jumpSrc	jlrSrc	retSrc	luiSrc	lliSrc	cgtSrc
NOOP	0000	0	0	0	000	0	1	1	0	0	0	0	0	0
ADD	0001	1	1	0	001	0	1	1	0	0	0	0	0	0
SUB	0010	1	1	0	010	0	1	1	0	0	0	0	0	0
NAND	0011	1	1	0	011	0	1	1	0	0	0	0	0	0
XOR	0100	1	1	0	100	0	1	1	0	0	0	0	0	0
SHL	0101	0	1	0	101	0	1	1	0	0	0	0	0	0
SHRA	0110	0	1	0	110	0	1	1	0	0	0	0	0	0
CGT	0111	1	1	0	010	0	1	1	0	0	0	0	0	1
SW	1000	x	0	1	001	1	x	1	0	0	0	0	0	0
LW	1001	0	1	1	001	0	0	1	0	0	0	0	0	0
BNQ	1010	x	0	0	010	0	x	0	0	0	0	0	0	0
LUI	1011	0	1	0	000	0	1	1	0	0	0	1	0	0
LLI	1100	0	1	0	000	0	1	1	0	0	0	0	1	0
JLR	1101	0	1	0	000	0	1	1	1	1	0	0	0	0
J	1110	x	x	x	000	x	x	1	1	0	0	0	0	0
RET	1111	x	0	x	000	x	x	1	0	0	1	0	0	0

Pipelined Processor Timing

add: 80 ns
sub: 80 ns
cgt: 70 ns
XOR: 55 ns
lui: 50 ns
lli: 50 ns
nand: 50 ns
shl: 50 ns
shra: 50 ns
sw: 80 ns
lw: 80 ns

Critical Path: 80 ns